FINAL REPORT FOR THE CENIIT PROJECT 01.05

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PROJECT TITLE

Design and implementation of digital signal processing systems
(Konstruktion och implementering av digitala signalbehandlande system)

DESIGN AND IMPLEMENTATION OF DIGITAL SIGNAL PROCESSING (DSP) SYSTEMS

BACKGROUND

The future society foresees globally interconnected digital communication systems offering delivery of information at any time, any place, and in any form. In this context, high-performance analog/digital interfaces and energy-efficient circuits are paramount. Another aspect that is becoming increasingly important is flexibility in the sense that different functions should be reconfigurable in order to suit communication systems that incorporate several different standards. This introduces the need for efficient multimode circuits that feature both flexibility and low energy consumption.

LONG-TERM GOAL

The energy consumption of DSP integrated circuits (ICs) is affected by decisions taken at all steps in the design and implementation process, from system level down to circuit and transistor level. This project studies the parts concerning the choice of DSP algorithms, a choice that has a large impact upon the energy consumption. The goal is to find new efficient DSP algorithms, in particular algorithms required in communication systems like filtering, signal reconstruction, estimation, etc. There is a distinction between DSP functions and DSP algorithms. A function is the task of the system whereas the algorithm says *how* we are going to implement this function. For example, a filter is a function, whereas a large number of algorithms exist that implement the same filter function. Algorithms that implement these functions mainly consist of a number of arithmetic operations, most of them being multiplications and additions. It is desired to find *efficient algorithms* (*low-complexity algorithms*) that require as few arithmetic operations as possible, as this in the end minimizes the device size and energy consumption, provided that algorithm dedicated ICs (as opposed to general-purpose DSP processors) are used which is the underlying assumption here. The number of operations can be substantially reduced by using a "smart" algorithm instead of a "straightforward" algorithm. The reason is that a straightforward algorithm most often contains redundant (unnecessary) computations. However, it is usually far from trivial to identify and remove this redundancy.

A main goal of this project has been to attain a fundamental knowledge of the computational properties of different DSP algorithms for important DSP functions. A key is to identify and remove redundant computations which leads to more efficient algorithms and in the end energy-efficient circuits. It should be noted though that there are also other factors, such as data communication and control, that contribute to the power consumption. It is thus important to reduce the number of arithmetic operations and memory accesses in such a way that the cost to implement the additional circuitry (control devices etc.) is not increasing, or at least increases less that the reduction gained by using a more efficient algorithm. In the proposed new algorithms, this is done by using similar structures as conventional ones regarding additional circuitry but that require less arithmetic operations and memory accesses. In this way, one will end up with an implementation with lower energy consumption.

The project is interdisciplinary in the sense that it considers both communication and digital signal processing (DSP) problems. It is common that "communication people" and "DSP people" work in parallel rather than together. Bringing different disciplines together is fruitful in order to come up with new innovative solutions. A long-term goal has been to continue along this path and to build up a research group that brings together communications and DSP. It is important to have such research groups since there is a lack of people covering two or several different areas.

RESEARCH RESULTS

Numerous new low-complexity DSP algorithms for different purposes have been developed during the project. We divide the research into seven main lines of work as described below.

1) Signal reconstruction

This part is on reconstruction of nonuniformly sampled bandlimited signals. We have proposed a new technique for reconstructing periodically nonuniformly sampled signals that is based on so called fractional delay digital filters. Compared to other techniques to this end, our approach has the following advantages: 1) the distortion can be made arbitrarily small by properly designing the digital fractional delay filters, 2) if properly implemented, the digital filters need not be redesigned in case the sampling pattern is changed. It suffices to adjust a few multiplier coefficient values that are determined by the sampling pattern. A (minor) disadvantage of this approach is that we need to use a certain amount of oversampling. This work has resulted in one journal paper [1], three conference papers [18], [20], [24] and one patent [94], acquired by Ericsson. Further, major parts of this work are included in the doctoral thesis of Dr. Per Löwenborg [68] who graduated in December 2002 and was supervised by the applicant.

Generalizing our system above, one ends up with reconstruction of general irregular (with some mild restrictions though) nonuniformly sampled bandlimited signals using time-varying filters. Such reconstruction algorithms find applications in several areas, e.g., mitigation of certain types of errors in analog-to-digital converters. We have recently shown how to design the time-varying filters in a proper manner. The advantages of this technique, over the one above, are 1) it can handle general irregularly nonuniformly sampled signals, 2) it offers a reduced implementation cost in those cases where the sampling pattern is not changed (or changes rarely), 3) it requires a smaller amount of oversampling. This work has resulted in one journal paper [8] and two conference papers [42], [44]. A problem of this approach is however that it requires on-line filter design whenever the sampling pattern is changed. To solve this problem, we have introduced different types of polynomial-based time-varying filters published in one journal paper [14] and two conference papers [54], [58].

2) Adjustable filters

This part concerns filters with adjustable frequency responses. We have developed a new design technique for adjustable fractional-delay FIR filters that leads to a reduced complexity [2], [21]. These filters are suitable for the first reconstruction technique discussed above. Another line of work has been on digital filters with adjustable bandwidth(s). Such filters find applications in e.g. Software-Defined Radio where interpolation and decimation with adjustable factors need to be handled. We have studied the problem of satisfying general specifications including passband and stopband edges for a whole set of specifications [35], [39]. Traditionally, only the passband edges (or stopband edges) have been controlled. Further, we have introduced a linear programming design technique for a class of adjustable-bandwidth linear-phase FIR filters which reduces the overall complexity compared to previously existing design techniques [9], [34], [41]. We have also showed that a bank of fixed overdesigned filters can reduce the complexity compared to techniques that use one filter with adjustable coefficients [6]. We have also proposed new structures for realizing efficient adjustable integer sampling rate converters [7], [40]. In a recent work, we have proposed a two-rate approach for reducing the complexity of adjustable fractional-delay FIR filters [52], [57], [63]. This approach leads to a complexity that is even lower than the single-rate approaches in [2], [21]. Another recent work is the introduction of complex adjustable fractional-delay FIR filters that can be used as a Hilbert transformer and fractional-delay filter at the same time [15].

3) Digital filters and two-channel filter banks

This work is on different types of digital filters and two-channel filter banks suitable for different specifications and applications. We have introduced several new efficient low-delay filters, interpolation and decimation filters, multirate filters, *M*th-band filters, and two-channel filter banks. Parts of this work have been done in co-operation with Prof. Tapio Saramäki of Tampere University of Technology in Finland. This work has resulted in four journal papers [3]–[5], [13] and eight conference papers [19], [23], [25], [26], [28], [30], [37], [38]. The paper [4] received the best paper award in *J. Circuits, Syst., Comp., Special Issue on Frequency-Response Masking Technique*, 2003.

4) Modulated *M*-channel filter banks

This part is on frequency selective *M*-channel filter banks which find application in e.g. communication systems where they are used as multiplexers and demultiplexers. The applicant's work in this area covers supervision of Dr. Linnéa Rosenbaum (earlier Svensson) who received her Doctoral degree in June 2007 [71] The thesis proposes new classes of so called modulated filter banks with lower complexity than previous such types of filter banks. This work has resulted in one journal paper [12] and six conference papers [22], [27], [29], [32], [31], [33]. The conference paper [31] received the best paper award of that conference.

5) Estimation and synchronization algorithms

This part concerns development of new robust and efficient estimation and synchronization algorithms for communication systems. The project leaders work in this area covers supervision of the Ph.D. student Mattias Olsson who finished his Licentiate degree in May 2006 [70]. This work has also resulted in seven conference papers [46], [49], [51], [53], [56], [59], [64].

6) Flexible frequency-band reallocation and transmultiplexer networks

This work is on flexible frequency-band reallocation (redirection-of-information) and transmultiplexer networks. Together with Per Löwenborg, the applicant has invented a new technique for flexible frequency-band reallocation based on new classes of flexible complex-modulated filter banks. The new technique outperforms previously existing techniques when all the aspects flexibility, low complexity and inherent parallelism, and perfect frequency-band reallocation are considered simultaneously. This work has so far resulted in one journal paper [11] and three conference papers [47], [60], [66]. Recent work has also been devoted to flexible transmultiplexers utilizing the Farrow structure and published in one journal paper [17] and two conference papers [65], [67].

7) High-performance analog/digital interfaces

This part is on high performance analog/digital interfaces (ADIs). It has become evident during the past years that the ever increasing requirements on ADIs as to the data rates and resolution most likely cannot be met by further progress in analog circuit topologies and technologies alone. To make radical improvements, it appears necessary to find new principles incorporating digital signal processing (DSP) algorithms. A fundamental concept that can be foreseen to be shared between all such principles is parallelization which is the natural way to increase the data rate. Our work in this area follows two different lines.

7.A) *Time-interleaved A/D converters.* One line of work is on time-interleaved A/D converters where M converters are used in parallel to increase the effective sampling rate by a factor of M. A problem of such converters is however that the parallelization introduces channel mismatch errors that must be estimated and compensated for by DSP algorithms. Together with Per Löwenborg, the applicant has developed new efficient estimation and correction algorithms that outperform previously existing ones. The new techniques incorporate adjustable/adaptive fractional-delay filters for the estimation and the algorithms discussed under 1) above for the correction (reconstruction). Parts of this work are covered in topic 5) above ([56], [59], [64]). This work has also resulted in the spin-off company Signal Processing Devices Sweden AB, one patent [94] and four patent applications [95]–[98].

7.B) *Parallel $\Sigma\Delta$ converters.* A second line of work is on parallel $\Sigma\Delta$ converters which are used to increase the relatively low bandwidth of single $\Sigma\Delta$ converters. A result of this work is a new general formulation of parallel $\Sigma\Delta$ converters in terms of circulant and pseudocirculant matrices derived from multirate filter bank theory, published in one journal paper [16] and one conference paper [62]. This formulation has not been utilized in this context before, but it turns out to be very powerful as it can be used to analyze the behavior of a practical overall ADC with channel gain, offset, and modulation sequence level mismatches present. This provides new insights that are very useful, not only for analysis of existing schemes, but also for the derivation of new ones. In particular, the new formulation gives us information about a particular scheme's sensitivity to the different channel mismatch errors. From this, one can deduce that many schemes in fact do not need "full calibration" to eliminate nonlinear distortion (aliasing), which earlier has been the common belief. It suffices to compensate for a subset of the different errors involved, which eases the calibration substantially. Another result is on complexity issues of decimation filters for ΣΔ converters published in a conference paper [61].

PROMOTIONS AND THESES

During the project, the project leader has been promoted to Docent (2001) and Professor (2004). Further, the project has generated two doctoral degrees [68], [71] and two licentiate degrees [69], [70]. A third doctoral degree is expected during 2008 (Mattias Olsson).

FINAL-YEAR PROJECTS

Final-year projects (examensarbeten) within the project include [72]–[75].

USE OF FUNDING

The project has mainly financed the project leader and to some minor extent the Ph.D. students involved. The Ph.D students have mainly been financed by SSF and VR.

INDUSTRIAL COOPERATION

The industrial co-operation has mainly been done through the spin-off company Signal Processing Devices Sweden AB, which is a result from the research described under topic 7.A above. The applicant and Per Löwenborg are two of the co-founders of this company. Products that utilize results in this project are under way. The company has at present about 20 employees.

CO-OPERATION WITH OTHER CENIIT PROJECTS AND INTERNATIONAL RESEARCH GROUPS

The applicant co-operates with Per Löwenborg as to research topic six and seven above. Per Löwenborg is funded by CENIIT for the project “Flexible frequency band reallocation”. As to other research groups, the main co-operation partner has up to now been Prof. Tapio Saramäki and his group at Tampere University of Technology in Finland as evidenced by several joint publications. More recently, we have also initiated a co-operation with Ewa Hermanowicz at Gdansk University of Technology in Poland and Christian Vogel at Graz University of Technology in Austria, also evidenced by joint publications.

RESEARCH GROUP

Within the division of Electronics Systems, the project leader supervises a group of Ph.D. students that mainly work on efficient design and implementation of DSP systems. At present, six Ph.D. students are supervised.

The people that have been involved in the project from 2001-2007 are:

Prof. Håkan Johansson (project leader)
Dr. Per Löwenborg (graduated 2002)
Dr. Linnéa Rosenbaum (graduated 2007)
Ph. D. Student Mattias Olsson (will graduate 2008)
Ph. D. Student Anton Blad
Ph. D. Student Amir Eghbali

PUBLICATIONS

Journal papers

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Conference papers

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