Final Report

Project title: **Design of Heterogeneous Embedded Systems with Distributed Hardware/Software Components**

Project leader: Petru Eles

Project started: January 1999

Project Report

1. Project Summary

This research deals with system-level design methods and tools for mixed hardware/software systems, with special emphasis on real-time issues. It is integrated as a part of ESLAB's research in the area of engineering techniques for time and safety critical embedded computer systems.

The aim of the research is to develop hardware/software codesign techniques for real-time applications. This entails formulating a hardware/software architecture model, developing a strategy to map a real-time system specification into such an architecture, and elaborating methods and tools for the analysis of a given design based on the given architecture. We also study the problem of how to use the analysis results to guide the modification of the given architecture in such a way that the final architecture corresponds to a near-optimal implementation of the system specification. Another important goal is the development of methods and tools for the verification of a design in the context of time-constrained systems.

The research work was done in cooperation with the industry, in particular with partners from Saab, Volvo Technological Development, and Ericsson. The research is also relevant, in general, for the industrial sector which develops embedded computer systems. Such systems make use of both off-the-shelf microprocessors and ASICs to implement specialized functions and have a very wide range of applications, including process control and computer-integrated manufacturing systems, transportation systems (automotive control, train control, ship control, and traffic control), avionics systems, missile control systems, telephone and communications systems, medical instruments, and different microcomputer-controlled domestic appliances.

We are interested to develop hardware/software codesign techniques for real-time applications implemented as distributed embedded systems. This is related to the common characteristics of embedded systems, namely that they must behave correctly both in terms of function and timing. In order to guarantee that both the function and timing of an embedded system are correct, extensive validation and verification are needed throughout the whole design and development process. Currently, much of this is done using traditional software testing and hardware simulation methods, but these are known to be inefficient and error prone. Further, these methods can only be efficiently used in the later stages of the design process when the detailed design has mostly been done. This results in a situation that the early design decisions, such as architecture selection, hardware/software partitioning, process scheduling, etc., which have high impact on the timing characteristics and cost of the final implementation, are made based on inadequate analysis of the designed system. Therefore, many problems are created early and discovered late when traditional methods are used.

One of the main cornerstones of our research is the fact that, due to increasing complexity, the design process has to move towards a methodology in which relatively complex blocks are reused and combined in order to deliver the required functionality (instead of designing from scratch). With such a design process, the focus is on the interaction of components and, in particular, on interfaces, protocols and glue logic which interconnect independent components allowing them to behave in a coherent way and to perform the required functionality.

2. Scientific Results

2.1 Specification, scheduling, and communication synthesis for distributed embedded systems

In order to capture both the data-flow and the control aspects of a given application, a conditional process graph representation has been defined. Algorithms for static, time-driven scheduling of

conditional process graphs on distributed systems have been developed and implemented. [1, 3]

The Time-Triggered Protocol (TTP) is becoming more and more accepted as the communication infrastructure for safety-critical automotive applications. In this context we have extended our scheduling algorithm, considering TTP as the particular protocol for inter-processor communication. At the same time, we have developed algorithms in order to optimize the parameters of the protocol such that specific requirements and constraints imposed by the application are met. [1, 2, 4, 5]

The results mentioned above, have been extended in order to be applied to systems with priority-based preemptive scheduling. This concerns both aspects related to scheduling of systems with data and control dependencies and the optimisation of the communication infrastructure. [8, 9, 10]

This research is highly significant for automotive applications and has been conducted in cooperation with Volvo Technical Development, Göteborg.

After the second year of the project (2000) this research direction has been continued, successfully, in the context of two other projects financed by SSF.

2.2 Modeling, analysis, and formal verification of real-time embedded systems

We have developed a formally based methodology for specification, analysis, and verification of real-time embedded systems. In this context a Petri-net based representation (called PRES+) has been proposed. Based on this representation and on model checking of hybrid automata, we have developed a methodology which allows to formally verify reachability and timing properties of the design. In addition, a simulation tool has been implemented, based on the PRES+ model. [6, 11, 12, 13]

Many efforts where concentrated towards improvement of the verification efficiency of PRES+ models, such that larger, real-life applications can be handled. Our solutions, in this regard, are based on two methods:

1. A transformational approach aimed at reducing the system model into a simpler but semantically equivalent one, which is consequently less time consuming to be verified.
2. A translation procedure from PRES+ into timed automata that significantly benefits the efficiency of the verification process by exploring the intrinsic concurrency of the model.

A radar jammer from Saab-Bofors Dynamics has been successfully used as a case study. [15, 17, 18, 19, 27]

There is very few work worldwide concerning the integration of a component-based design process with formal verification. In this context, we have proposed a component based design methodology which includes not only aspects related to communication synthesis but also formal verification. The approach is based on the PRES+ notation. The basic idea is that systems are build using pre-verified components which are interconnected using glue logic, protocol adapters, etc. The challenge is to verify that the whole system is performing according to specifications.

We have developed the underlying theoretical framework and have implemented a tool support for verification. A methodology for the modelling of the interconnected components has been developed. The approach has been validated by case studies. [20, 26, 36, 37].

2.3. Analysis and optimisation of soft real-time systems

One important input we got from our industrial partners, in particular from Ericsson Radio Systems, is that performance estimation and scheduling (as part of the system design process) based on deterministic worst case execution times is not a realistic approach for their application area.

Therefore, we proposed two approaches to handle soft real time systems. One is a probabilistic approach, while the other is based on soft tasks with utility functions.

We have developed an approach to analytical performance estimation of systems where the task execution times are known probabilistically. Schedulability analysis of stochastic tasks raises additional challenges compared to classical worst-case execution time task models. We addressed the problem under as general assumptions as possible. As an underlying mathematical model for the analysis, we use stochastic processes, in particular, generalized semi-Markov chains. [16].

Due to complexity reasons, the above approach can only be applied to the analysis of monoprocessor systems. The multiprocessor case is intrinsically more difficult to treat than the monoprocessor one, due to the true parallelism and inter-processor communication. Therefore, in a second approach, we offer the possibility of certain trade-offs between complexity of the solution (in terms of time and memory) and precision. The approximation implies that real-world execution time probability distribution functions (ETPDF) are approximated with Coxian distributions with a designer-specified accuracy. This solution allows the designer to trade analysis accuracy for analysis speed and memory demand. The experimental setup we used to assess the applicability of our approach included parts of the baseband digital signal processing of a GSM basestation from Ericsson Radio Systems. [21, 22, 29, 30].

Once the analysis tools described above were available, we have continued the work towards design space exploration and system optimisation in the context of applications with stochastic task execution times. The main challenge, in this context, consists in the huge complexity of the analysis which is guiding the design space exploration process. A design space exploration approach emphasizing task mapping with quality constraints expressed as percentage of missed deadlines, has been developed. [39]

In the context of soft real-time systems we also considered the problem of quasistatic scheduling of systems composed of both hard an soft real-time tasks. In order to capture the relative importance of soft tasks and how the quality of results is affected when missing a soft deadline, we use utility functions associated to soft tasks. Thus, our objective is to find a schedule that maximizes the total utility and, at the same time, guarantees hard deadlines. Such an approach allows for an accurate modelling of a large class of applications where quality of service is defined in a more complex way then just by hard deadlines. Since a purely off-line solution is too pessimistic and a purely on-line approach incurs an unacceptable overhead due to the high complexity of the problem, we have proposed a quasi-static approach where a number of schedules are prepared at design-time and the decision of which of them to follow is taken at run-time, based on the actual execution times. We developed both an exact algorithm as well as different heuristics to solve the problem [32, 33, 38].

2.4 Energy optimisation of time constrained embedded systems

Considering also suggestions from our industrial partners, during the fourth project year (2002) we have started to work on energy optimisation of real-time embedded systems. This is an extremely important topic in the context of current developments in the electronic and VLSI industry. Our main focus is system-level power minimization, in particular scheduling policies with dynamic voltage scaling. The main emphasis of this work is on [23, 24, 25, 28, 31, 34, 35, 40]:

1. Taking into consideration not only dynamic power consumption but also leakage power for dynamic voltage scaling. In current and future technologies, leakage power is becoming more and more significant for the global power budget. However, researchers have neglected this aspect for system level optimizations.
2. Optimization of the communication infrastructure with particular emphasis on the power consumption aspect.
3 Development of dynamic, on-line voltage scaling approaches with a very low time and energy overhead.

3. Promotions and Examina Related to the Project

Petru Eles

1999 - Docent
2002 - Professor

Paul Pop

2000 - Licentiate: “Scheduling and Communication Synthesis for Distributed Real-Time Systems”

2003 - PhD: “Analysis and Synthesis of Communication-Intensive Heterogeneous Real-Time Systems“

Luis Alejandro Cortes

2001 - Licentiate: “Verification of Real-Time Embedded Systems using Petri Net Models and Timed Automata“

2005 - PhD: “Verification and Scheduling Techniques for Real-Time Embedded Systems“ (Defense on March 2, 2005).

Sorin Manolache

2003 - Licentiate: “Schedulability Analysis of Real-Time Systems with Stochastic Task Execution Times"

Daniel Karlsson

2003 - Licentiate: “Towards Formal Verification in a Component-based Reuse Methodology“

4. Master Thesis Related to the Project

1. Daniel Karlsson, “A Front End to a Java based Environment for the Design of Embedded Systems”, 2000.
2. John Alexandersson, “Real-Time Operating Systems for Embedded Applications. From Literature to Real-life”, 2000.
3. Daniel Forsgren, “System Level Instruction Set Simulation of the Alpha Architecture”, 2001.
4. Oskar Blomberg, “Modelling and Simulation of Real-Time Systems with Discrete and Continuous Behaviour”, 2001.
5. Roger Kantrup, “Building Large and Scalable Distributed Systems: A Method Based on Per-

formance Modelling", 2002.
6. Magnus Ekhall, "Simulation Framework for the 802.11 MAC", 2002.
7. Liwen You, "Evaluation of Message-Oriented Middleware", 2002.
8. Antoiane Haddad, "Development of a Real-Time Multi-Sensor Data Acquisition and Tracking System", 2002.
9. Johan Segertoft & Björn Westman, "Robust Functionality in Vehicles", 2002.
10. Henrik Friman, "Petri Net Class Library and Translation from PRES+ to Timed Automata", 2003.
11. Johannes Petersson, "A Flexible Simulator for Control-dominated Distributed Real-Time Systems", 2003.
12. Fabien Lambergeon, "C++ Analysis Library for Real-Time Embedded Systems Modelled with Deterministic and Stochastic Colored Petri Nets", 2003.
13. Naidu Sriharsha Charan Reddy, "Automatic Environment Generation for Formal verification of Component-based Systems", 2003.
14. Jirong Zhu, "Towards an Extensible Visual Editor for Embedded Systems representation Models", 2003.
15. Xiaobo Wang, "Design and Implementation of a Tool for Modeling, Simulation and Verification of Component-based Embedded Systems", 2004.

5. People Financed from the Project

The research work has been coordinated by Petru Eles, who has been partially financed from the project.

PhD Students involved and partially financed over the years:

1. Paul Pop
2. Sorin Manolache
3. Luis Alejandro Cortés
4. Daniel Karlsson.
5. Alexandru Andrei

6. Industry Contacts

The work has been performed in cooperation with the following industrial partners:

Volvo Technological Development.
The work on scheduling and communication synthesis for distributed embedded systems has been performed in cooperation with Volvo Technological Development (contact persons: Jakob Axelsson, Henrik Lönn, Magnus Hellring). The student working on this project, Paul Pop, has spent several weeks at Volvo TD. An automatic cruise controller has been used as a case study.

Saab-Bofors Dynamics.
The work on formal verification using the PRES+ notation has been performed in cooperation with Saab-Bofors Dynamics (contact persons: Peter Lind, Stefan Kvist). A radar jammer is used as a case study.

Ericsson.
The work on performance estimation with stochastic execution times (contact persons: Erik Stoy, Jonas Plantin) and the research concerning communication based design and verification (contact persons: Dan Lindqvist, Björn Fjellborg) have been performed in cooperation with Ericsson. Sor-

in Manolache, one of the PhD students involved, has spent several weeks at Kista and worked on a case study based on the GSM Base Transceiver Station.

7. Research Group

Dr. Petru Eles has been employed at Linköping University in 1998 as universitetslektor. The present project has provided the financing needed for him to start his research work. Based on first results, further research funding has been obtained. At present, prof. Petru Eles is the main adviser for seven PhD students which are part of the Embedded Systems Laboratory at IDA.

8. Publications related to the project

1. P. Eles, A. Doboli, P. Pop, Z. Peng, *Scheduling with Bus Access Optimization for Distributed Embedded Systems*, IEEE Transactions on VLSI Systems, vol. 8, No 5, October 2000, pp. 472-491.
2. P. Pop, P. Eles, Z. Peng, *Schedulability-Driven Communication Synthesis for Time Triggered Embedded Systems*, 6th International Conference on Real-Time Computing Systems and Applications (RTCSA'99), Hong Kong, 1999, pp. 287-294.
3. P. Pop, P. Eles, Z. Peng, *An Improved Scheduling Technique for Time-Triggered Embedded Systems*, 25th Euromicro Conference, Milan, Italy, 1999, pp. 303-310.
4. P. Pop, P. Eles, Z. Peng, *Communication Scheduling for Time-Triggered Systems*, 11th Euromicro Conference on Real-Time Systems, York, England, 1999 (Work in Progress Proceedings).
5. P. Pop, P. Eles, Z. Peng, *Scheduling with Optimized Communication for Time-Triggered Embedded Systems*, 7th International Workshop on Hardware/Software Codesign Rome, Italy, 1999, pp. 178-182.
6. L. A. Cortes, P. Eles, Z. Peng, *A Petri Net Based Model for Heterogeneous Embedded Systems*, IEEE NORCHIP Conference, Oslo, Norway, 1999, pp. 248-255.
7. R. Jigorea, S. Manolache, P. Eles, Z. Peng, *Modelling and Simulation of Heterogeneous Embedded Systems with UML*, IEEE International Symposium on Object-oriented Real-time Distributed Computing (ISORC 2000), Newport Beach, California, 2000, pp. 210-213.
8. P. Pop, P. Eles, Z. Peng, *Performance Estimation for Embedded Systems with Data and Control Dependencies*, 8th International Workshop on Hardware/Software Codesign, San Diego, 2000, pp. 62-66.
9. P. Pop, P. Eles, Z. Peng, *Bus Access Optimization for Distributed Embedded Systems Based on Schedulability Analysis*, Design Automation and Test in Europe (DATE2000), Paris, March, 2000, pp. 567-574.
10. P. Pop, P. Eles, Z. Peng, *Schedulability Analysis for Systems with Data and Control Dependencies*, 12th Euromicro Conference on Real-Time Systems, Stockholm, Sweden, 2000, pp. 201-208.
11. L.A. Cortes, P. Eles, Z. Peng, *Verification of Embedded Systems using a Petri Net based Representation*, 13th International Symposium on System Synthesis (ISSS 2000), Madrid, Spain, 2000, pp. 149-155.
12. L.A. Cortes, P. Eles, Z. Peng, *Formal Coverification of Embedded Systems using Model Checking*, 26th Euromicro Conference, Maastricht, The Netherlands, 2000, 106-113.
13. L. A. Cortes, P. Eles, and Z. Peng, *Definitions of Equivalence for Transformational Synthesis of Embedded Systems*, Intl. Conference on Engineering of Complex Computer Systems (ICECCS), Tokyo, Japan, 2000, 134-142.

14. D. Karlsson, P. Eles, Z. Peng, *A Front End to a Java Based Environment for the Design of Embedded Systems*, 4th IEEE DDECS Workshop, Gyor, Hungary, 2001, pp. 71-78.
15. L. A. Cortes, P. Eles, Z. Peng, *Hierarchical Modeling and Verification of Embedded Systems, Euromicro Symposium on Digital Systems Design*, Warsaw, Poland, 2001, pp. 63-70.
16. S. Manolache, P. Eles, Z. Peng, *Memory and Time-Efficient Schedulability Analysis of Task Sets with Stochastic Execution Time*, 13th Euromicro Conference on Real-Time Systems, Delft, The Netherlands, 2001, pp. 19-26.
17. L.A. Cortes, P. Eles, Z. Peng, *Verification of Real-Time Embedded Systems using Petri Net Models and Timed Automata*, Proceedings of the 8th International Conference on Real-Time Computing Systems and Applications (RTCSA 2002), Tokyo, Japan, 2002, pp. 191-199.
18. M. Varea, L.A. Cortes, B. Al-Hashimi, P. Eles, Z. Peng, *Symbolic Model Checking of Dual Transition Petri Nets*, Proceedings of the 10th International Symposium on Hardware/Software Codesign (CODES 2002), Estes Park, Colorado, 2002, pp. 43-48.
19. L.A. Cortes, P. Eles, Z. Peng, *An Approach to Reducing Verification Complexity of Real-Time Embedded Systems*, 14th Euromicro Conference on Real-Time Systems, Vienna, Austria, 2002 (Work in Progress Proceedings), pp. 45-48.
20. D. Karlsson, P. Eles, Z. Peng, *Formal Verification in a Component-based Reuse Methodology*, Proceedings of the 15th International Symposium on System Synthesis (ISSS 2002), Kyoto, Japan, 2002, pp. 156-161.
21. S. Manolache, P. Eles, Z. Peng, *Schedulability Analysis of Multiprocessor Real-Time Applications with Stochastic Task Execution Times*, Proceedings of the 20th IEEE/ACM International Conference on Computer Aided Design (ICCAD 2002), San Jose, California, 2002, pp. 699-706.
22. S. Manolache, *Schedulability Analysis of Real-Time Systems with Stochastic Task Execution Times*, Licentiate thesis, Linköping University, 2002.
23. D. Wu, B. Al-Hashimi, P. Eles, *Scheduling and Mapping of Conditional Task Graph for the Synthesis of Low Power Embedded Systems*, Proceedings of Design, Automation & Test In Europe (DATE 2003) Conference, Munich, Germany, 2003, pp 90-95.
24. M. Schmitz, B. Al-Hashimi, P. Eles, *A Co-Design Methodology for Energy-Efficient Multi-Mode Embedded Systems with Consideration of Mode Execution Probabilities*, Proceedings of Design, Automation & Test In Europe (DATE 2003) Conference, Munich, Germany, 2003, pp 960-965.
25. M. Schmitz, B. Al-Hashimi, P. Eles, *Iterative Schedule Optimisation for Voltage Scalable Distributed Embedded Systems*, ACM Transactions on Embedded Computing Systems, vol. 3, Nr. 1, 2004, pp. 182-217.
26. D. Karlsson, Formal Verification in a Component-Based Reuse Methodology, Licentiate thesis, Linköping University, 2003.
27. L.A. Cortes, P. Eles, Z. Peng, *Modeling and Formal Verification of Embedded Systems Based on a Petri Net Representation*, Journal of Systems Architecture, vol. 49, no. 12-15, December 2003, pp. 571-598..
28. D. Wu, B. Al-Hashimi, P. Eles, *Scheduling and Mapping of Conditional Task Graph for the Synthesis of Low Power Embedded Systems*, IEE Proceedings - Computers & Digital Techniques, Vol. 150, Issue 5, September 2003, pp. 303-312.
29. S. Manolache, P. Eles, Z. Peng, *Schedulability Analysis of Applications with Stochastic Task Execution Times*, ACM Transactions on Embedded Computing Systems, Vol. 3, No. 4, November 2004, pp. 706-735
30. S. Manolache, P. Eles, Z. Peng, *An Approach to Performance Analysis of Multiprocessor Applications with Stochastic Task Execution Times*, submitted for publication.
31. M. Schmitz, B. Al-Hashimi, P. Eles, *Co-Synthesis of Energy-Efficient Multi-Mode Embedded Systems with Consideration of Mode Execution Probabilities*, IEEE Transactions on CAD of

Integrated Circuits and Systems, accepted for publication.
32. L.A. Cortes, P. Eles, Z. Peng, *Static Scheduling of Monoprocessor Real-Time Systems composed of Hard and Soft Tasks*, DELTA 2004 (International Workshop on Electronic Design, Test and Applications), Perth, Australia, 2004, pp. 115-120.
33. L.A. Cortes, P. Eles, Z. Peng, *Quasi-Static Scheduling for Real-Time Systems with Hard and Soft Tasks*, Design Automation and Test in Europe Conference (DATE2004), Paris, France, pp. 1176-1181.
34. A. Andrei, M. Schmitz, P. Eles, Z. Peng, B. Al-Hashimi, *Overhead-Conscious Voltage Selection for Dynamic and Leakage Energy Reduction of Time-Constrained Systems*, Design Automation and Test in Europe Conference (DATE2004), Paris, France, pp. 518-523.
35. A. Andrei, M. Schmitz, P. Eles, Z. Peng, B. Al-Hashimi, *Simultaneous Communication and Processor Voltage Scaling for Dynamic and Leakage Energy Reduction in Time-Constrained Systems*, International Conference on Computer Aided Design (ICCAD 2004), San Jose, USA, November 7-11, 2004, pp. 362-269.
36. D. Karlsson, P. Eles, Z. Peng, *A Formal Verification Approach for IP-based Designs*, Forum on Specification and Design Languages, Lille, France, September 13-17, 2004, pp. 556-567.
37. D. Karlsson, P. Eles, Z. Peng, *A Formal Verification Methodology for IP-based Designs*, Euromicro Symposium on Digital System Design, Rennes, France, August 31-September 3, 2004, pp 372-379.
38. L.A. Cortes, P. Eles, Z. Peng, *Combining Static and Dynamic Scheduling for Real-Time Systems*, Workshop on Software Analysis and Development for Pervasive Systems (SONDA 2004), Invited Paper, Verona, Italy, August 24, 2004, pp. 32-40.
39. S. Manolache, P. Eles, Z. Peng, *Optimization of Soft Real-Time Systems with Deadline Miss Ratio Constraints*, 10th IEEE Real-Time and Embedded Technology and Applications Symposium, Toronto, Canada, May 2004, pp. 562-570.
40. A. Andrei, M. Schmitz, P. Eles, Z. Peng, B. Al-Hashimi, Quasi-Static Voltage Scaling for Energy Minimization with Time Constraints, Design Automation and Test in Europe Conference (DATE 2005), Munich, 2005, accepted for publication.